



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,860	07/13/2006	Nigel P. Smith	NAN155 US	7177
34036 7590 03/16/2010 Silicon Valley Patent Group LLP 18805 Cox Avenue Suite 220 Saratoga, CA 95070				
EXAMINER MIYOSHI, JESSE Y				
ART UNIT		PAPER NUMBER		
2811				
MAIL DATE		DELIVERY MODE		
03/16/2010		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/549,860

Applicant(s)

SMITH ET AL.

Examiner

JESSE Y. MIYOSHI

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 and 26-30 is/are pending in the application.
- 4a) Of the above claim(s) 7 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-21 and 26-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB-08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 1, 2, 9, 10, 14, 15, 21, 28-30 are objected to because of the following informalities:

2. Claim 1, lines 12 and 13; claim 2 line 2; claim 10 line 2; claim 14 line 2; claim 15 line 3; claim 21 line 15; claim 28 lines 9 10 12, 14; claim 29 line 2 and 3; and claim 30 lines 4 and 7 uses the term "the mark structure" or "the rectangular mark structure" or "elongate rectangular test structure" or "elongate rectangular sub-structure" which should be "the elongate rectangular mark structure".
3. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-6, 8-11, 16-21, and 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Adel et al. (U.S. PGPub 2003/0026471; hereinafter "Adel").

Re claim 1: Adel teaches (e.g. figure 9 and paragraph 103) an overlay metrology mark for determining the relative position between two or more layers of an integrated

circuit structure comprising a first mark portion (**132A**, **132D**, **132E**, **132H**) associated with a first layer (**132A** and **D** disposed in the first layer; **132E** and **H** are disposed in the first layer; e.g. paragraph 103) and a second mark portion (**132B**, **132C**, **132F**, **132G**) associated with a second layer (**132B** and **C** disposed in the second layer; **132F** and **G** are disposed in the second layer; e.g. paragraph 103), wherein the first (**132A**, **132D**, **132E**, **132H**) and second mark portions (**132B**, **132C**, **132F**, **132G**) together constitute, when the mark is properly aligned, at least one pair of test zones (**134**), each test zone comprising a first mark section (**132A**, **132E**) formed as part of the first mark portion (**132A**, **132D**, **132E**, **132H**) and a second mark section (**132B**, **132F**) formed as part of the second mark portion (**132B**, **132C**, **132F**, **132G**) each mark section comprising a plurality of elongate rectangular mark structures (**138A**, **138B**) in parallel array adjacently disposed to form the said test zone (**134**), the plurality of elongate rectangular mark structures (**138A**, **138B**) of the first mark section (**132A**, **132E**) and the plurality of elongate rectangular mark structures (**138A**, **138B**) of the second mark section (**132B**, **132F**) are positioned side by side in a direction that is perpendicular to a direction of measured displacement between the first mark section (**132A**, **132E**) and the second mark section (**132B**, **132F**), such that the mark structures (**138A**, **138B**) in a first test zone (upper left **134**) are substantially at 90° with respect to the mark structures (**138A**, **138B**) of at least one other test zone (upper right **136**), and wherein the test zones making up the at least one pair of test zones (upper left **134** and upper right **136**) are laterally displaced relative to each other along at least one of a first direction

(horizontal direction) and an orthogonal second direction (vertical direction) by a distance great enough to avoid errors in measurement caused by proximity effects.

Re claim 2: Adel teaches an overlay metrology mark wherein the mark structures (**138A**, **138B**) in each test zone (upper left **134** and upper right **136**) are laterally disposed relative to each other such as in use to have mirror symmetry about an imaging axis of the imaging apparatus.

Re claim 3: Adel teaches an overlay metrology mark wherein each mark portion is developed within or on the said layer (**132A** and **D** disposed in the first layer; **132E** and **H** are disposed in the first layer, **132B** and **C** disposed in the second layer; **132F** and **G** are disposed in the second layer; e.g. paragraph 103).

Re claim 4: Adel teaches an overlay metrology mark wherein each mark portion is printed on the said layer by a microlithographic process (photolithographic techniques; e.g. paragraph 42).

Re claim 5: Adel teaches an overlay metrology mark wherein each test zone (upper left **134** and upper right **136**) has a generally square or rectangular outline shape (square shape), the axes of the square or rectangular shape corresponding to the said first and second directions and to mirror axes of the imaging equipment in use (axis along the meeting faces of **138B** between **132E** and **132F**).

Re claim 6: Adel teaches an overlay metrology mark wherein test zones (upper left **134** and upper right **136**) are generally square.

Re claim 8: Adel teaches an overlay metrology mark comprising more than one pair of test zones (**134** is “**pair one**”; **136** is “**pair two**”), wherein each pair is laterally disposed equidistantly about a common center in one or other of the said two directions.

Re claim 9: Adel teaches an overlay metrology mark comprising a one pair (**pair one**) disposed in a first direction and another pair (**pair two**) in a second direction.

Re claim 10: Adel teaches an overlay metrology mark wherein the first (**132A, 132E**) and second (**132B, 132F**) mark sections of each zone comprise closely adjacent mark structures (**138A, 138B**) in parallel array in a common direction, respectively part of the first mark portion (**132A, 132D, 132E, 132H**) and the second mark portion (**132B, 132C, 132F, 132G**), and wherein the first (**132A, 132E**) and second (**132B, 132F**) mark sections of two zones (**134, 136**) are in the first direction (**138A** are horizontally positioned) and the first (**132D, 132H**) and second (**132C, 132G**) mark sections of the other two zones (**134, 136**) in similar arrays but disposed at right angles thereto (**138B** are vertically positioned), and the two test zones (**134, 136**) in each pair are laterally spaced in respectively an X and Y direction about common centers.

Re claim 11: Adel teaches an overlay metrology mark wherein the elongate rectangular mark structures (**138A, 138B**) comprise single monolithic rectangular structures.

Re claim 16: Adel teaches an overlay metrology mark wherein the pitch of the elongate rectangular mark structures is of constant period in each mark section (**138A, 138B** have constant pitch).

Re claim 17: Adel teaches an overlay metrology mark wherein the period is identical in all mark sections (all marks are disposed vertically or horizontally).

Re claim 18: Adel teaches an overlay metrology mark wherein all elongate rectangular mark structures (**138A**, **138B**) in a test zone have identical widths and spacing.

Re claim 19: Adel teaches an overlay metrology mark wherein each elongate rectangular mark structure has a width of around 0.5 to 2 μm (0.2 μm ; e.g. paragraph 77), and wherein spacing between elongate rectangular mark structures in the array is between 1/2 and two structure widths.

Re claim 20: Adel teaches an overlay metrology mark wherein each mark section comprises at least five elongate rectangular mark structures (**138A**, **138B**) in each direction.

Re claim 21: Adel teaches (e.g. figure 9 and paragraph 103) a method for providing an overlay metrology mark to determine the relative position between two or more layers of an integrated circuit structure comprises the steps of: laying down a first mark portion (**132A** and **D** disposed in the first layer; **132E** and **H** are disposed in the first layer; e.g. paragraph 103) in association with a first layer; and laying down a second mark portion (**132B** and **C** disposed in the second layer; **132F** and **G** are disposed in the second layer; e.g. paragraph 103) in association with a second layer; the first (**132A**, **132D**, **132E**, **132H**) and second (**132B**, **132C**, **132F**, **132G**) mark portions being so structured as to together constitute, when the mark is properly aligned, at least one pair of test zones (upper **134** and upper **136**), each test zone (**134**,

136) comprising a first mark section (**132A**, **132E**) formed as part of the first mark portion (**132A**, **132D**, **132E**, **132H**) and a second mark section (**132B**, **132F**) formed as part of the second mark portion (**132B**, **132C**, **132F**, **132G**) each mark section comprising a plurality of elongate rectangular mark structures (**138A**, **138B**) in parallel array adjacently disposed to form the said test zone (**134**, **136**), the plurality of elongate rectangular mark structures (**138A**, **138B**) of the first mark section (**132A**, **132E**) and the plurality of elongate rectangular mark structures (**138A**, **138B**) of the second mark section (**132B**, **132F**) are positioned side by side in a direction that is perpendicular to a direction of measured displacement between the first mark section (**132A**, **132E**) and the second mark section (**132B**, **132F**), such that the mark structures (**138A**, **138B**) in each test zone (**134**, **136**) are in alignment within the test zone, said alignment being in a first direction (horizontal) in half of the test zones (**134**) and in a second direction (vertical) substantially at 90° thereto in the other test zones (**136**), and wherein the test zones (**134**, **136**) making up the at least one pair of test zones (upper **134** and upper **136**) are laterally displaced relative to each other along at least one of the said first direction (horizontal) and said second direction (vertical direction) by a distance great enough to avoid errors in measurement caused by proximity effects.

Re claim 26: Adel teaches the method, wherein the first (**132A**, **132D**, **132E**, **132H**) and second (**132B**, **132C**, **132F**, **132G**) mark portions are so structured as to together constitute, when the mark is properly aligned, more than one pair of test zones (**134**, **136**), wherein each pair is laterally disposed equidistantly about a common center in at least one of the said first and second directions.

Re claim 27: Adel teaches the method, wherein the first (132A, 132E) and second (132B, 132F) mark sections of each test zone (134, 136) comprise closely adjacent mark structures (138A, 138B) in parallel array in a common direction, respectively part of the first mark portion (132A, 132D, 132E, 132H) and the second mark portion (132B, 132C, 132F, 132G), and wherein the first (132A, 132E) and second (132B, 132F) mark sections of two zones (134) are in the first direction (horizontally) and the first (132A, 132E) and second (132B, 132F) mark sections of the other two zones (136) in similar arrays but disposed at right angles thereto, and the two test zones (134, 136) in each pair are laterally spaced in respectively an X and Y direction about common centers.

Re claim 28: Adel teaches (e.g. figure 9 and paragraph 103) an overlay metrology mark for determining the relative position between two or more layers of an integrated circuit structure, the overlay metrology mark comprising at least a pair of test zones (134, 136), the test zones being laterally displaced relative to each other by a distance great enough to avoid errors in measurement caused by proximity effects, each test zone (134, 136) comprising a first mark section (132A and D disposed in the first layer; 132E and H are disposed in the first layer; e.g. paragraph 103) formed on a first layer of the integrated circuit structure and a second mark section formed on a second layer (132B and C disposed in the second layer; 132F and G are disposed in the second layer; e.g. paragraph 103) of the integrated circuit structure, the second layer being disposed over the first layer, each of the mark sections (132A,D,E,H and 132B,C,F,G) comprising a plurality of parallel elongate rectangular mark structures

(138A, 138B), wherein when the overlay metrology mark is properly aligned the mark structures in the first mark section (132A,D,E,H) are parallel to and adjacently disposed to the mark structures in the second mark section (132B,C,F,G) and the long axis of each rectangular mark structure (138A, 138B) of the first mark section (132A,D,E,H) is collinear with a long axis of a corresponding rectangular mark structure (138A, 138B) of the second mark section (132B,C,F,G) within each test zone (134, 136) and are perpendicular with respect to the rectangular mark structures in the other test zone (134, 136).

Re claim 29: Adel teaches the overlay metrology mark comprising four test zones (134, 136), wherein the long axis of each rectangular mark structure (138A, 138B) of the first mark section (132A,D and 132E,H) is collinear with a long axis of each rectangular mark structure (138A, 138B) of and the second mark section (132B,C and 132F,G) along a first direction in a first test zone (upper 134) and a second test zone (upper 136) and are collinear along a second orthogonal direction in a third test zone (lower 134) and a fourth test zone (lower 136).

Re claim 30: Adel teaches the overlay metrology mark, comprising four test zones (upper 134, upper 136, lower 134, lower 136), wherein a first test zone (upper 134) and a second test zone (lower 134) are aligned on an axis along a first direction (horizontal direction) and are separated by a distance that is approximately equal to a total length of the rectangular mark structures in both the first mark section (132A,D,E,H) and the second mark section (132B,C,F,G) of a third test zone (upper 136), and wherein the third test zone (upper 136) and a fourth test zone (lower 136) are

aligned on an axis along a second direction (vertical direction) that is orthogonal to the first direction (horizontal direction) and are separated by a distance that is approximately equal to a total length of the rectangular mark structures (**138A**, **138B**) in both the first mark section (**132A,D,E,H**) and the second mark section (**132B,C,F,G**) of the first test zone (upper **134**).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adel and further in view of Ballarin (U.S. 6,876,092).

Re claim 12: Adel teaches substantially the entire claimed structure of claim 1 as recited above except explicitly stating an overlay metrology mark wherein the elongate rectangular mark structures comprise arrangements of substructures constituting together a general elongate rectangular outline.

Ballarin teaches (e.g. figure 2) an overlay metrology mark wherein the elongate rectangular mark structures (**3**) comprise arrangements of substructures (**23**, **25**) constituting together a general elongate rectangular outline (**3**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ballarin in the device of Adel in order to enable a more accurate measure of overlay errors (see column 7, lines 52-53 of Ballarin).

Re claim 13: Adel modified by Ballarin teaches overlay metrology mark wherein the elongate rectangular mark structures (3) comprises a row or column as the case may be of smaller constituent test structures (23, 25), for example a row or column of squares.

Re claim 14: Adel modified by Ballarin teaches an overlay metrology mark wherein each elongate rectangular test structure (3) and/or each constituent test structure comprise arrangements of design rule sized sub-structures (23, 25).

Re claim 15: Adel modified by Ballarin teaches an overlay metrology mark wherein the arrangements of design rule sized sub-structures (23, 25) are selected from parallel arrays of elongate rectangular sub-structures in either direction, arrays of square sub-structures (23, 25), circles in square or hexagonal array, arrays of holes within a suitably shaped test structure and any combinations of these or other like patterns.

Response to Arguments

8. Applicant's arguments with respect to claim 1-6, 8-21, and 26-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **JESSE Y. MIYOSHI** whose telephone number is (571)270-1629. The examiner can normally be reached on **M-F 7:30AM-5:00PM EST**. Alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jesse Miyoshi/

/Ori Nadav/
Primary Examiner, Art Unit 2811